CAPACITOR VOLTAGE BALANCING CONTROL OF CASCADED MULTI-LEVEL INVERTER FOR POWER QUALITY CONDITIONER

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Abstract- Multilevel inverter technology has emerged recently as a very important alternative in the area of high power medium-voltage energy control. In all multilevel technology, cascade multilevel inverters have become the major circuits used in power quality conditioners. Evidently the voltage balancing problem of DC capacitors of cascade inverters is a key problem to the power quality conditioners. This paper explores voltage balancing control fundament. This paper mainly focuses on capacitor voltage balancing of cascaded multi-level inverter based on proposed novel algorithm. The proposed work can be simulated using MATLAB/SIMULINK and the performance with level shifted carriers and phase shift carriers can be presented and analyzed. The simulation and experiment results illustrate that the voltage of each capacitor is controlled and balanced while working.

Keywords- cascaded multi-level inverter, dc voltage balancing control, power quality conditioner,

I.INTRODUCTION

In recent years, the demand for high-power ac power supplies with low harmonic distortion has been continuously increasing. Among the various converters, multilevel converters attract a lot of attention. The series connection of multilevel converter modules reduces the voltage stress of each switch in the single-phase full-bridge (H-bridge) module, making the multilevel converters suitable for high power applications [1–4]. The multilevel converters synthesizing the output voltage with step pulses can produce output voltages with less harmonic distortion by using advanced modulation strategies [3]. Power quality problems have been discussed a lot for quite a long time because of the widespread use of nonlinear electronic equipments. To provide high power quality at the point of common coupling (PCC) of a distribution system, Power quality conditioner, including voltage regulation, reactive power and harmonic compensation is widely used and researched in the Power engineering field nowadays [1-3]. But due to the limitation of voltage capability of the present power devices, it is very difficult to handle the nonlinear loads in high voltage grid using the traditional power quality conditioner with two-level inverter. When the cascade multilevel inverter is applied to the power quality conditioner, each of the cascaded H-bridge inverters is equipped with an isolated DC capacitor without any power, source. To make the equipment work properly, each DC capacitor voltage must be maintained high enough and balance. The number of output voltage levels in the conventional cascaded multilevel inverter is defined by M=2S+1,, where s is the number of dc voltage sources. However, tolerances of passive components, unequal conducting and switching losses produced by power switching devices, and parameter imbalance in the control circuit will cause voltage imbalance to DC capacitors in an actual system. Voltage balancing problem, which is an inherent problem of cascade multilevel topology, restricts the development and application to power quality conditioners.

The control algorithm is analyzed and compared the THD based on a phase-shifted carrier modulation and level shift carrier modulation strategies. Presently, various strategies of balancing each DC bus voltage have been presented by researchers. But no literature analyzes theoretically between the charge and discharge process of each H-bridge DC capacitor and. the switching states of the equipment. The small-signal model for analyzing DC capacitor voltage balance control hasn't be set up. This paper explores voltage balancing control fundament. A model based on output pulses of H-bridge inverters utilizing voltage switching functions is developed as a means to investigate the control law and to offer a more intuitive insight into the problem. Then based on the analysis and the model, a novel capacitor voltage balancing method is proposed. Presently, various strategies of balancing each DC bus voltage have been presented by researchers. But no literature analyzes theoretically between the charge and discharge process of each H-bridge DC capacitor and. the switching states of the equipment. The simulation

results illustrate that the voltage of each capacitor is also controlled and balanced while working.

II. PRINCIPLE OF CASCADED MLTI-LEVEL INVERTER STRUCTURE OF POWER QUALITY CONDITIONER

The structure of the power quality conditioner with cascade multilevel inverter is shown in Fig.1. Nonlinear load (NL) produces periodic non-sinusoidal current. Desired current of the power quality conditioner is injected into the power system by controlling the cascade PWM inverters to achieve voltage regulation, reactive power and harmonic compensation. Fig.1shows that each phase of this equipment consists of two H-bridge inverter units. U_{dc_a1} and U_{dc_a2} are DC flying capacitor voltages of the two H-bridge units of A phase respectively. The H-bridge inverter is built-up of four switches, each one with its freewheeling diode. The states of T_1 and T_3, T_2 and T_4 are complementary. The switch T_1 is closed, whilst the other T_3 is opened at every time instant. The allowed logic configuration of switches of the H-bridge inverter can produce four switching States. The H-bridge inverter is able to provide the three different output voltage values. The general function of this cascade multilevel inverter is to synthesize a desired voltage from output voltage of each H-bridge inverter of each phase.

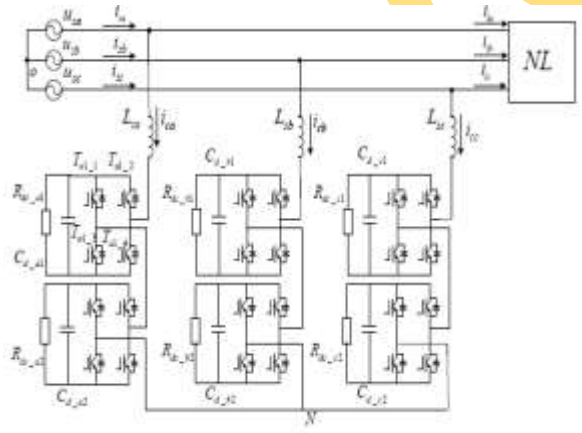

Fig.1 Schematic diagram of power quality conditioner With cascade multilevel inverter

To analyze DC capacitor voltage balancing problem, we use an equivalent resistance in parallel with dc flying capacitor to represent all the losses of each H-bridge unit. The losses include switching losses produced by power switching devices and losses of DC capacitors. In Fig.1, $Rdc_{\_i1}$ and R_{dc_i2}(i=a,b,c) are Resistances of the two H-bridge units respectively, C_{d_i1} and C_{d_i2} (i =a, b,c) are capacitors of the two H-bridge units respectively. The power losses on the inductance L_{si} (i=a, b, c) are represented with an equivalent resistances Rsa (i=a, b, c). The switching state of the first H-bridge of phase A, S_{a1} of power devices T_{a1_1} - T_{a1_4}, is defined as S_{a1}=1 when power devices T_{a1_1} and T_{a1_4} are switched on; S_{a1}=-1 when power devices T_{a1_2} and T_{a1_3} are switched on; S_{a1}=0 when power devices T_{a1_1} and T_{a1_2} are switched on or T_{a1_2} and T_{a1_4} are switched on, which is shown as follows:

$$S_{a1}=\begin{cases} 1, T_{a1\_1}, T_{a1\_4}\ ON\ and\ T_{a1\_2}, T_{a1\_3}\ OFF \\ 0, T_{a1\_1}, T_{a1\_2}\ ON\ and\ T_{a1\_3}, T_{a1\_4}\ OFF \\ -1, T_{a1\_2}, Ta1_3\ ON\ and\ T_{a1\_1}, T_{a1\_4}\ OFF \end{cases} \quad (1)$$

The switch states are coded by symbols -1, 0 and 1 identifying the three voltage levels on each H-bridge inverter. According to explanations above, switching functions of the first and second H-bridge unit in phase A can be demonstrated by S_{a1} and S_{a2} respectively. Using the same method, S_{b1}, S_{b2}, S_{c1} and S_{c2} are obtained too. From the equation above, the following equation of the current and voltage relationship between dc part and ac part of the first H-bridge is easily got:

$$\begin{cases} U_{a1} = S_{a1}.U_{dc\_a1} \\ i_{dc\_a1} = S_{a1}.i_{ca} \end{cases} \quad (2)$$

U_{a1} is the output voltage of the first H-bridge, i_{a1} is the output current of the first H-bridge; i_{dc_a1} is the current flying through the DC flying capacitor. Theory analysis of voltage balancing control fundament will be explained [4]

III.MODULATING TECHNIQUES

The most widely used PWM schemes for multilevel inverters are the carrier-based level shift PWM (LSPWM) and phase shift techniques and the space vector PWM (SVPWM) technique [5].

A. Sinusoidal PWM

Pulse width modulation control is most widely used method of controlling the modulation depth of inverters, including the multilevel family. A significant amount of research has been published on the various ways of implementing PWM control. The focus here is on carrier-based sinusoidal PWM schemes for controlling a cascaded multilevel inverter. We consider only three very simple dispositions that seem the most interesting: All the carriers are phase disposition (PD), All the carriers above the zero value reference are in phase among them but in opposition with those below (POD)

and All the carriers are alternatively in opposition disposition (APOD)

B. Phase Disposition (PD)

In this method carriers are the same in frequency, amplitude and phases, but they are just different in DC offset to occupy contiguous bands as shown in Fig 2. The carriers are in phase across all the bands. For this technique, significant harmonic energy is concentrated at the carrier frequency, but since it is co-phasal component, it does not appear in the line-to-line voltage. Generation of gate pulses with triangular carriers [8]. the generation of gate pulses with triangular carriers of cascaded five-level inverter with R-load. In this four triangular carriers are selected on the basis of the formula m-1, i.e 5-1=4.

C. *Phase Opposition Disposition (POD)*

Carriers in this method are the same in frequency and amplitude but they are again different in phase and DC offset as the case of APOD. But in this method carriers above the reference zero point are out of phase with those below that by $180^{0.}$ Generation of gate pulses with triangular carriers [8].

D. *Alternative Phase Opposition Disposition (APOD)*

In this method carriers have the same frequency and the same amplitude but they are different in their DC offset and phases as shown in Fig.4. In this method carriers are phase shifted by 180^{0}, so this method uses two degrees of freedom of carriers namely their DC-offset and phases. generation of gate pulses with triangular carriers [8] Among the discussed techniques, PD technique has less harmonic distortion on line voltages. As it shown PD technique puts the harmonic energy directly into a common mode carrier component so that the harmonics are cancelled in line voltages.

E. Phase shifted PWM (PSPWM)

Phase shift PWM [5] involves the same principle of standard 2-level PWM to gate the switches using the comparison between two signals, reference and carrier, but exploit more than one carrier to generate the driving signals. The required carriers, all with the same amplitude and frequency, depend on the number of levels: in a converter with n levels**,** n −1 carriers are necessary. As the name suggests, the carriers have to be displaced, shifting their phases. The phase shift can be done choosing any delay, but the minimum harmonic distortion of the output is achieved using the delay Δ given by (3) where S T is the switching period.

$$\Delta = \frac{T_s}{n-1} \qquad (3)$$

IV. CAPACITOR VOLTAGE BALANCING ALGORITHM

First of all, the control block diagram of the whole system is given. The system combines harmonic current extraction, current tracking control, and capacitor voltage balancing control. The control block diagram of the whole system is shown in Fig.5. The method for detecting harmonic currents based on
The instantaneous reactive power theory is adopted. In order to control the shape of output current Waveform, PI control technology is adopted. The first two parts have been studied widely. The whole voltage control algorithm will be divided into two parts: the overall active power control and the individual voltage balance control [6]. In Fig.2, k represents the Number of the cascaded cell in cascaded multilevel inverter. The former control loop will keep the sum of each phase capacitor voltage equal to its setting value. The latter control loop makes capacitor voltage of each H-bridge unit equal.

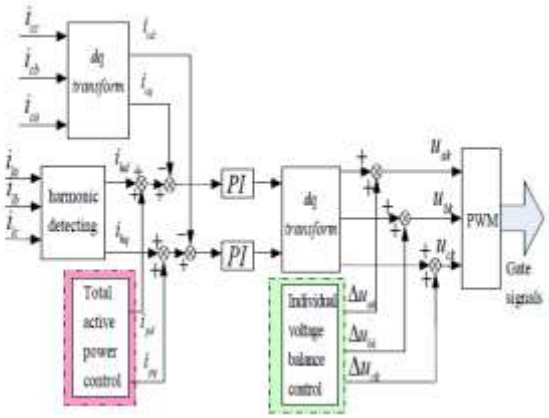

Fig.2 Control block diagram of the whole system

The principle of the overall active power control is the same as the traditional two level APFs and has been used widely [6]. So we won't discuss it in details here. Its control diagram [4].When the overall active power that needed to compensate all the losses of the whole system is controlled in the overall active Power control loop, the sum of each phase capacitor voltage is controlled to the set value. Then we need guarantee DC voltage of each H-bridge unit equal. Because the switching frequency is high, DC voltage variation of the unit in a switching cycle is very small to DC voltage value. So the loss of the equivalent resistance in parallel

with dc flying capacitor is approximately equal before and after regulation. if we want to change the active power absorbed by the H-bridge, we can't do other than to change output pulse phase φ_{a1} or width w_{a1} or both. It is clear that, the final composed results may be just the same as before after regulating width of each output pulse.That is to say, regulating width of output pulses to redistribute active power may not influence the final output of the equipment and can be used as effective method to balance DC voltages. By using individual Voltage balance control we can obtain the two capacitor voltages are equal to the set value and they are balanced in the each unit. its control block diagram [4].

V. SIMULATION RESULTS

In order to compare the performance of the control method simulation waveforms of capacitor voltages with or without DC voltage control loop are given. Theoretic analysis results are necessary to be further verified by the simulation. The diagrammatic sketch of simulation power circuits is as Fig.1. The parameters of the circuit for the simulation are: switch frequency is 10 kHz, DC capacitor is 3300uF and DC voltage of each H-bridge unit is supposed to Be equal to 400V respectively; the equivalent resistances, Rdc_i1 and Rdc_i2 (i=a, b, c), of the two units are different, Rdc_i1=150Ω, Rdc_i2=350Ω. Simulation waveforms are given as follows.

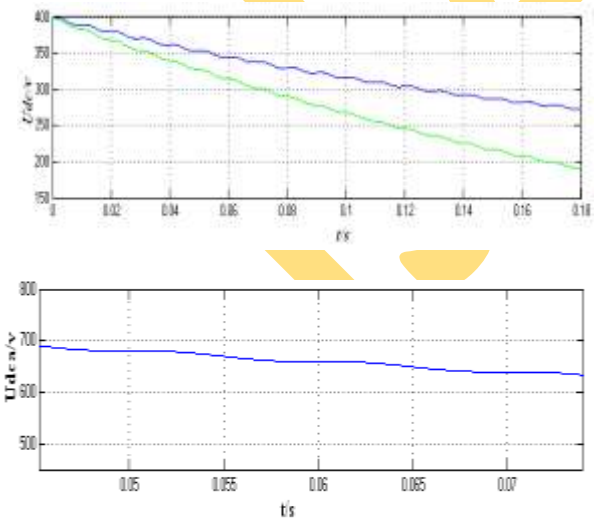

Fig.3 DC voltage waveforms when no voltage loops are added

When DC voltage control loop is not added, the two capacitor voltages are differ from each other and the sum of them is not equal to the set value, as shown in Fig.3 When the overall active power control loop is added while the individual voltage balance control loop is not added, the sum of the two capacitor voltages are equal to the set value but they are differ from each other, as shown in Fig.4.

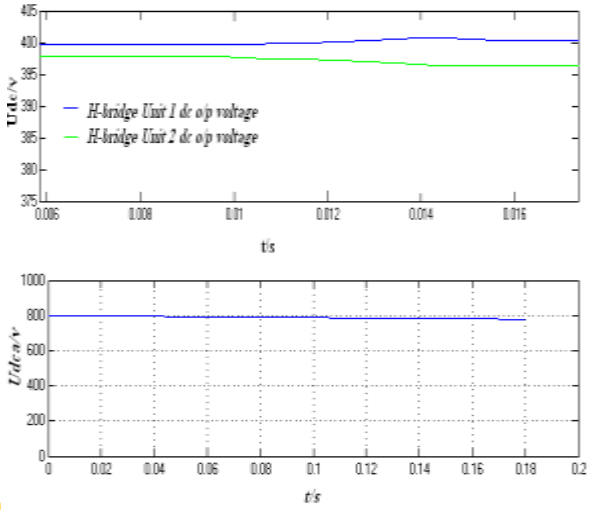

Fig.4 DC voltage waveforms when only the overall active power control loop is added

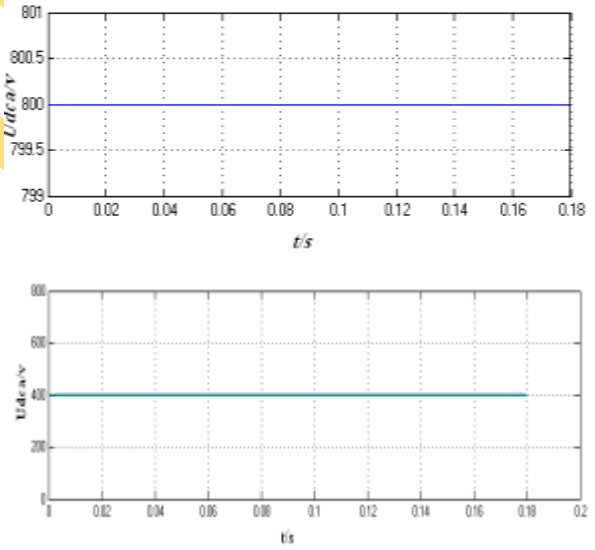

Fig5.DC voltage waveforms when DC voltage control loops are added

It can be seen that the two DC capacitor voltages fluctuate at the point of 400V and are simultaneously balanced in steady states. The proposed control method is effective and has good static state characteristics Fig5.AndFig.6 shows steady waveforms of load current and system supply current, where waveform 1 is the load current *il*, waveform 2 is system supply current *is*

through the power quality conditioner filtering. The THD (total harmonic distortion) of load current *il* is calculated to be 28.92%. The THD of *is* is 2.46%.

Table: 1 THD Comparison of Phase Shift and Level Shift PWM Techniques

Modulation Technique	Parameter	
	Source Current **(%THD)**	Load Current **(%THD)**
Phase shift PWM	2.46	28.92
Level shift PWM	7.24	29.46

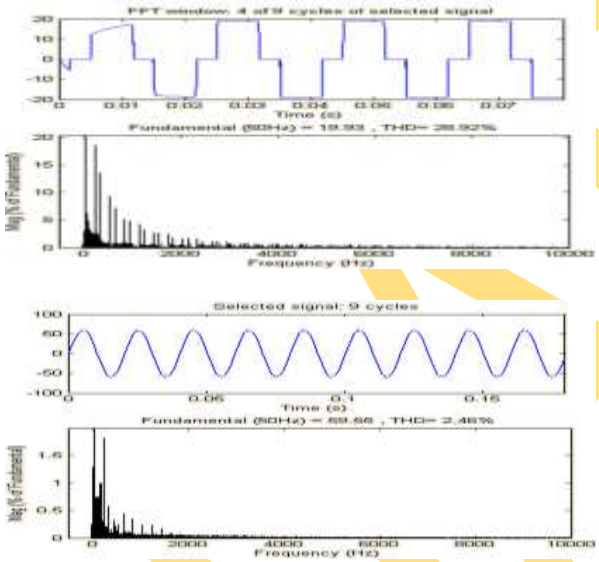

Fig.6 steady waveforms of load current and system supply current using phase shift carrier based PWM

VI. CONCLUSIONS

In this paper, DC capacitor voltage balancing problem is investigated for the power quality conditioner with cascade multilevel inverter. The issue of voltage balance is discussed from output pulses of H-bridge inverters point of view, and a new dc capacitor voltage balance method is proposed and proved by simulation and experiment results. The results illustrate that both the theory analysis and the control method are satisfactory. Moreover, the research by this paper may be applied to asymmetric cascaded multilevel converter with different DC voltages and different switching frequency too.

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